Preliminary data

Type	Ordering code
S 187	Q 67100–Y 199

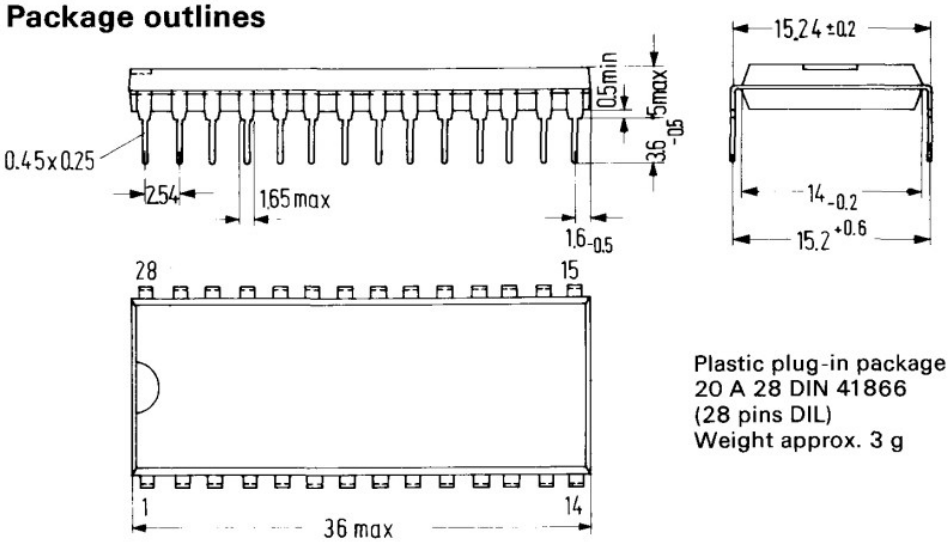
The S 187 is a highly integrated MOS-circuit in p-channel metal-gate technology with enhancement and depletion transistors, featuring the following special technical properties:

- More than 500 000 different frequencies pre-settable
- 8 different reference frequencies pre-settable
- High degree of flexibility through appropriate coding
- High reference input frequency
- Integrated phase comparator
- Simple 10 V supply
- Low power consumption even at high frequencies
- Usable together with diode matrix S 353

Application areas

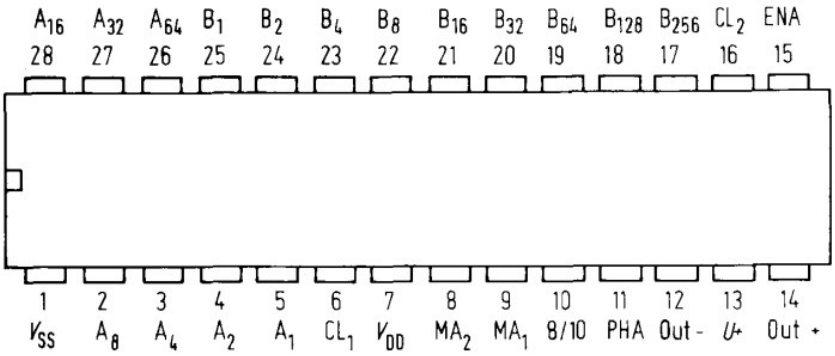
- Multichannel equipment
- Navigation equipment
- Citizen-band radio
- Scanning receiver
- Signal generators

Package outlines



Plastic plug-in package
20 A 28 DIN 41866
(28 pins DIL)
Weight approx. 3 g

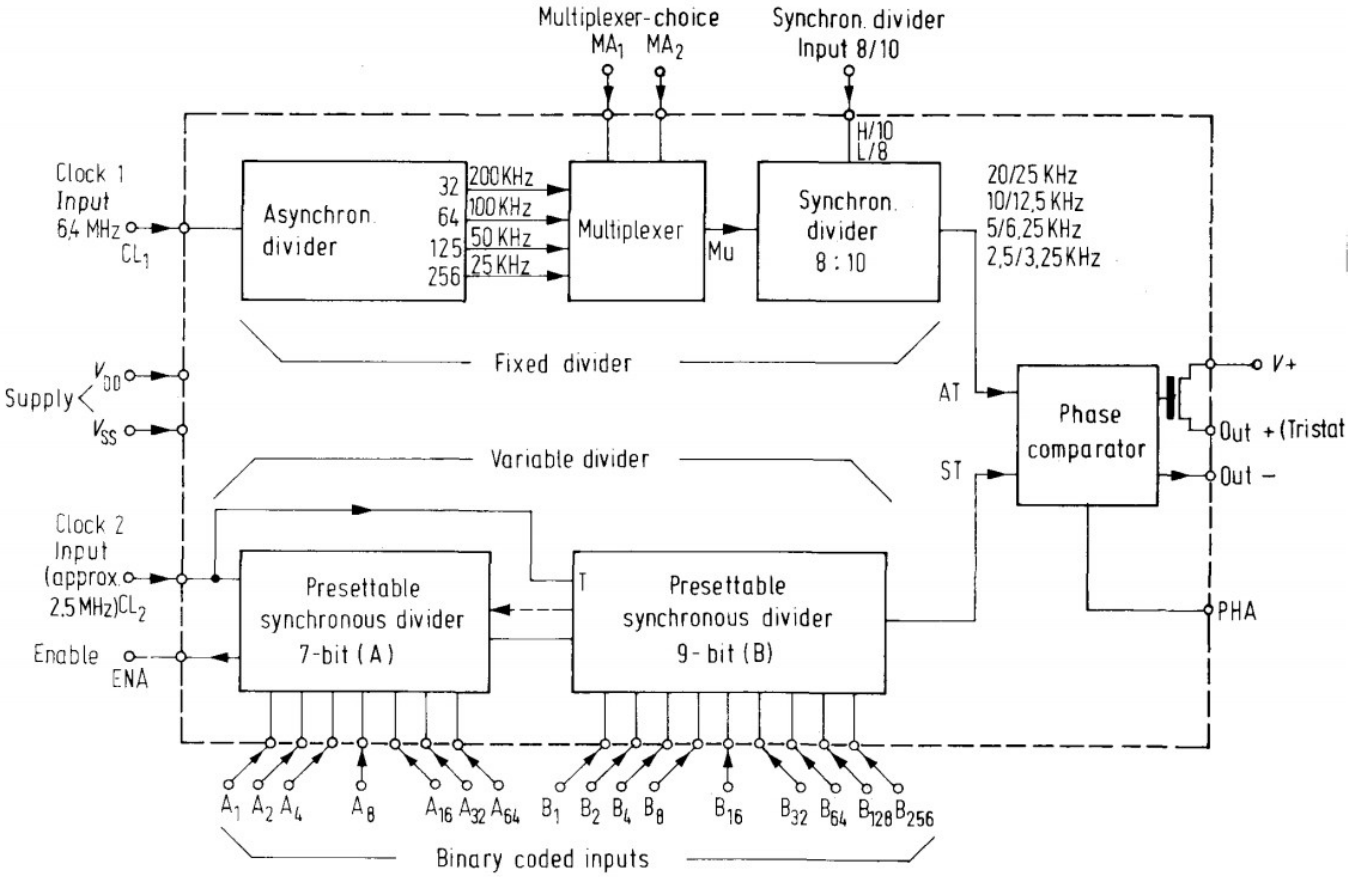
Pin connections, top view



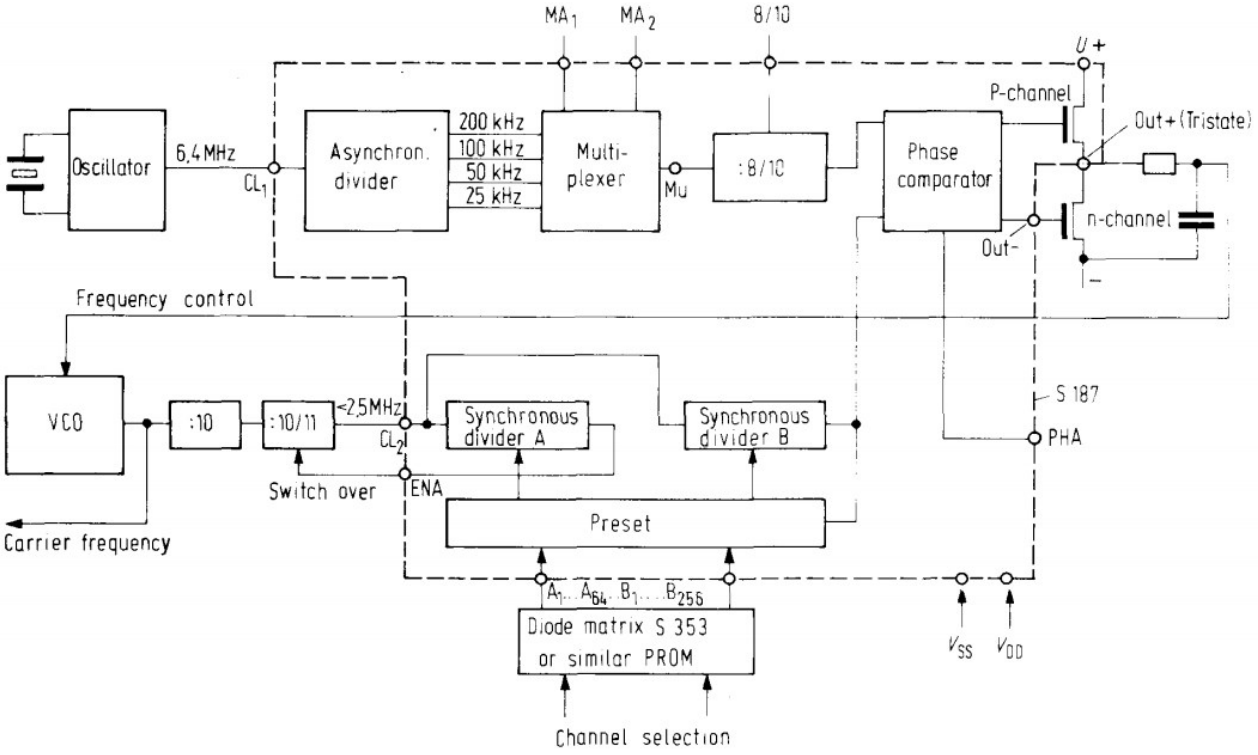
Pin designations:

Inputs			Outputs		
Abbrev.	Pin		Abbrev.	Pin	
A_1	5	Binary coded inputs for pre-settable synchronous divider (A) 7 bits	ENA	15	Release-output
A_2	4		PHA		Phase comparator output
A_4	3		out +	14	Output +
A_8	2		out −	12	Output −
A_{16}	28		$U+$	13	Output for the control of external u-channel transistor
A_{32}	27				
A_{64}	26				
B_1	25	Binary coded inputs for pre-settable synchronous divider (B) 9 bits			
B_2	24				
B_4	23				
B_8	22				
B_{16}	21				
B_{32}	20				
B_{64}	19				
B_{128}	18				
B_{256}	17				
CL_1	6	Clock input 1 for asynchronous divider (max. 6.4 MHz)			
CL_2	16	Clock input 2 for synchronous divider (max. 2.5 MHz)			
8/10	10	Divider setting 8 or 10 for asynchronous divider			
MA_1	9	Multiplexer choice 1 and 2			
MA_2	8				
V_{SS}	1	Supply voltages			
V_{DD}	7				

Block diagram



Block diagram of a carrier frequency generator with S 187



Maximum ratings

			Lower limit B	Upper limit A	Unit
Supply voltage Voltage at all pins	relative to V_{DD} = 0 V	V_{DD} V	15 V 15 V	−0.3 −0.3	V V
Input current (V_I = 0.3 V; V_{DD} = 0 V)		I_F		1	mA
Storage temperature		T_S	−55	+125	°C
Ambient operating temperature		T_{amb}	−20	+70	°C

Operating characteristics: (T_{amb} = 25°C)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	Used as common and reference voltage	0	0	V
Supply voltage $V_{SS\,typ}$ = 10 V	V_{SS}	V_{DD} = 0V	9	11	V
Current supply	I_{SS}	$I_{SS\,typ}$ = 8 mA		35	mA
Inputs A_1 through A_{64} B_1 through B_{256}, $^8/_{10}$)					
L-resistance	R_{IL}	C_{in} = 10 pF to V_{SS}	0	3	kΩ
H-resistance	R_{IH}	Current input "L" max = ≈ 500 µA (short circuit to V_{DD} at V_{SS} = 10 V)	100	∞	kΩ
Input CL_1					
L-input voltage	V_{IL}	$F_{Cl1\,max}$ = 6.5 MHz,	V_{DD}	V_{SS} −8	V
H-input voltage	V_{IH}	$t_a = t_f$ = 25 ns C_{in} = 15 pF to V_{SS} pulse duration 50 ns min.	V_{SS} −0.5	V_{SS}	V
Input CL_2					
L-input voltage	V_{IL}	$F_{CL\,2\,max}$ = 2.5 MHz,	V_{DD}	V_{SS} −8	V
H-input voltage	V_{IH}	$t_a = t_f$ = 50 ns C_{in} = 25 pF to V_{SS} pulse duration 150 ns min.	V_{SS} −0.5	V_{SS}	V

Operating characteristics: (T_{amb} = 25°C)

		Test conditions	Lower limit B	Upper limit A	Unit
Inputs MA_1, MA_2					
L-input voltage	V_{IL}	C_{in} = 10 pF	V_{DD}	V_{SS} −8	V
H-input voltage	V_{IH}	to V_{SS}	V_{SS} −0.5	V_{SS}	V
Outputs OUT+, OUT-					
L-output voltage	V_{QL}	I_L = 1 mA, V_{SS} = 10 V	9		V
H-output voltage	V_{QH}	I_H = −1 mA, V_{SS} = 10 V		4	V
	$I_{UK\ max}$	1 µA at T_{amb} = 70 °C			
Output PHA					
L-output voltage	V_{QL}	I_L = 100 µA, V_{SS} = 10 V		6.5	V
H-output voltage	V_{QH}	I_H = −1 mA, V_{SS} = 10 V	6.5		V
Output ENA					
L-output voltage	V_{QL}	open-drain			
H-output voltage	V_{QH}	I_H = 3.5 mA ECL-interface	5		V

Basic functions

The Frequency synthesizer S 187 is used for channel selection in the Carrier Frequency Generator. The carrier frequency is generated by a voltage-controlled oscillator (VCO) and after a **pre-set division** (depending on channel) compared with a crystal-stabilized reference frequency. The output voltage of the frequency comparator controls the VCO.

By appropriate choice of the division, the carrier frequency can be set to a particular multiple of the reference frequency.

Construction and function

See block diagram of a carrier frequency generator including the portion integrated in the S 187.

The following functions are comprised:

a) 8-stage asynchronous divider, input frequency 6.4 MHz max., output frequency selectable 200, 100, 50, 25 kHz.

b) switchable : 8/ : 10-divider,

a) and b) together supply the crystal-stabilized reference frequency (8 possibilities).

c) fully programmable synchronous divider consisting of two interconnected parts; input frequency $\leq$2.5 MHz;

1) 7-stage divider A, pre-settable from : 1 through : 127-division. After completion of the process this divider is stopped. It is reset and triggered by divider B. Consequently it generates the switching signal for a : 10/ : 11 pre-divider, which causes a nonius-kind of division; for this purpose the comparator frequency may be adjusted to a higher value. The switching signal (output ENA) must therefore be synchronized with the input clock (delay $<$300 nsec.).

2) 9-stage divider B, pre-settable from : 2 through : 512-division. At the end of the process this divider resets itself and divider A. It supplies the divided carrier frequency for the phase-comparator.

d) The phase comparator (see figure) performs the frequency comparison. It possesses 3 possible output combinations (see truth table 1) between which it switches, initiated by 0 → 1 transitions at the inputs (see truth table 2).

In the case of the input frequencies being different, the leading signal switches the output on its side (AT out +, ST out –) to "1"; it remains at this level until the other signal switches it back to "zero".

If both frequencies are equal but different in phase, an output pulse with the width of the phase difference is generated on the leading side with each clock pulse. In the case of both 0 → 1 transitions at the inputs lying within the dwell period, the phase comparator will remain in the "0"-state.

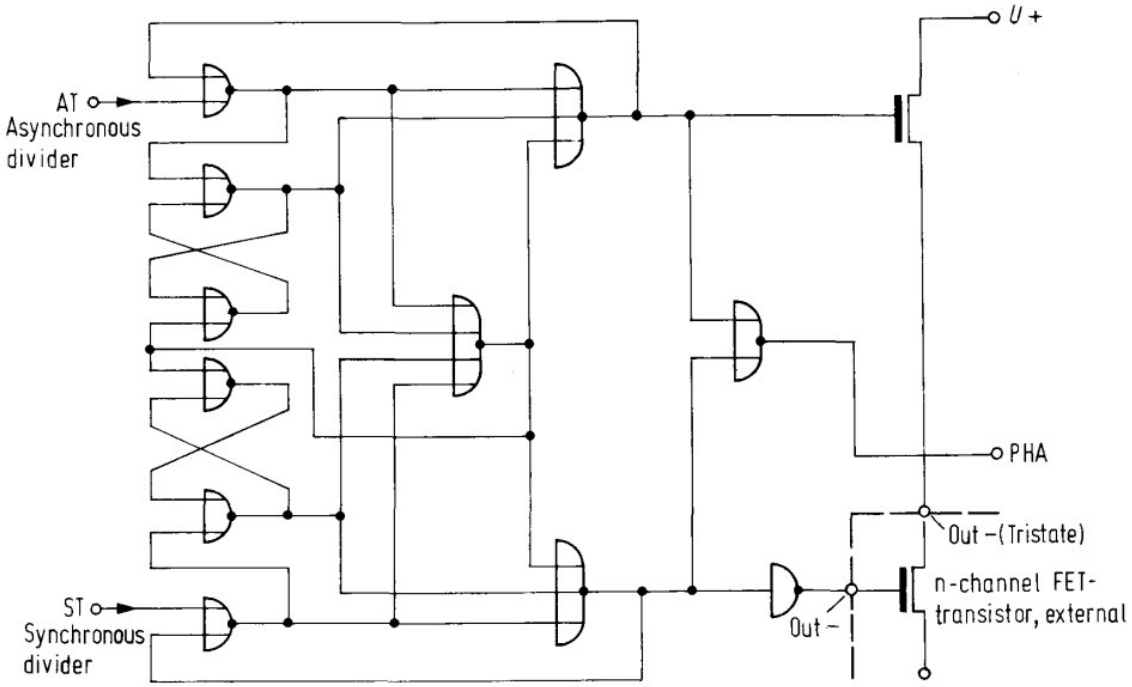
The phase comparator drives a complementary tristate gate, whereby the internal p-channel transistor is driven by the positive-output and the external n-channel transistor from the inverted negative-output. Consequently, the integration capacitor is charged during an H-level, discharged during an L-level. During a O-level its output is connected to a high resistance. Therefore the capacitor voltage, and consequently the frequency of the VCO, changes until the 0 → 1-transitions are within one dwell period of the phase comparator at both inputs.

e) Active-p-function of the programming inputs. The assignment of individual frequencies to particular speech-channels can be done, for example, using a 10 x 16 PROM (diode matrix), which connects the selected programming inputs through a low resistance with a negative potential (L), loading the not-selected ones only with leakage currents (H).

The equivalent worst-case values are: 5 kΩ to V_{DD} (L) or 100 kΩ to V_{DD} (H).

The programming inputs have therefore been provided with an active-p-circuit (see figure), which in the H-condition creates an input voltage of $> V_{SS} - 1$ V and in the L-condition an input voltage of $< V_{DD} + 1$ V. This way various ways of driving the inputs are made possible.

Phase comparator



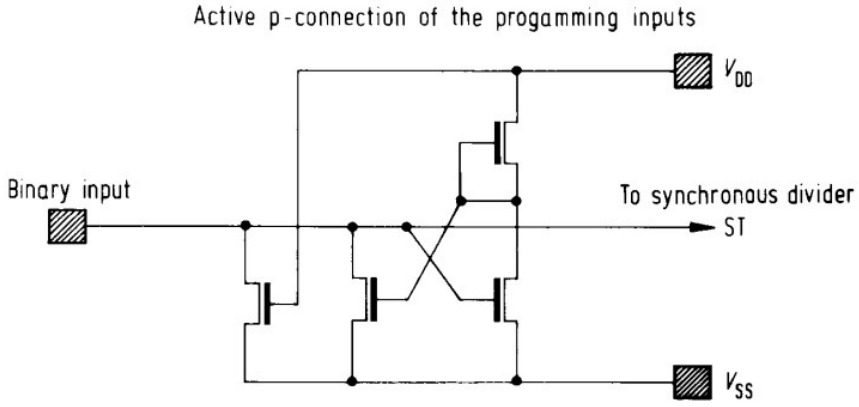
Truth table 1 Phase comparator

Condition PHA Phase comparator	Output +	Output –
H	1	0
L	0	1
0	0	0

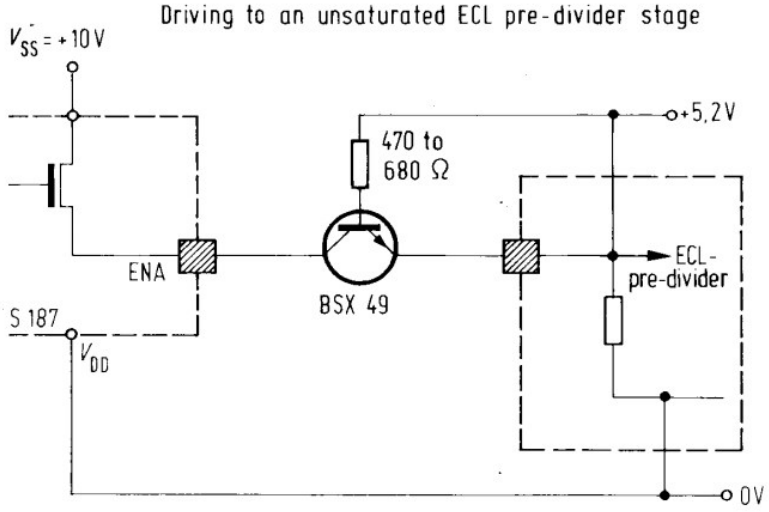
Truth table 2 Phase comparator

Output condition PHA Phase comparator	0 → 1-transition at	
	AT Asynchronous divider	ST Synchronous divider
H	H	0
0	H	L
L	0	L

Active-p-connection of the programming inputs



Driving an unsaturated ECL pre-divider stage



Truth tables of dividing ratios for synchronous divider (ST) and asynchronous divider (AT)

a) Inputs 8/10:

H	division by 10
L	division by 8

b) Inputs A_1 through A_{64}:

LSB = A_1
MSB = A_{64}

Condition H LLL LLL corresponds to division by 1

c) Inputs B_1 through B_{256}:

LSB = B_1
MSB = B_{256}

Condition H LLL LLL LL corresponds to division by 1

d) Inputs MA_1 and MA_2:

MA_1	MA_2	Frequency setting at MU
L	L	25 kHz
H	L	50 kHz
L	H	100 kHz
H	H	200 kHz